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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/654,920	09/05/2003	Mitsuyoshi Endo	02887.0248	6812

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EXAMINER	
SEMENENKO, YURIY	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/654,920	ENDO ET AL.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Amendment filed on 1/30/2006 has been entered.
In response to the Office Action dated 08/29/ 2005, Applicants has amended claims 2, 5 and 10-12. Claims 13-16 have been withdrawn from consideration as directed to non-elected claims.
Claims 1-16 are now pending in the application.

Response to Arguments

2. Applicant's arguments filed 5/09/2005 have been considered but are moot in view of the new grounds of rejection.

Specification

3. The disclosure is objected to because of the following informalities:
Page 1, line 28: there is not terminal electrodes 12 on Fig.1;
Appropriate correction is required.

Claim Objections

4. Claim 5 is objected to for improper antecedent. Claim recites the limitation "the junction". There is not such limitation in claim 1. There is insufficient antecedent basis for this limitation in claim 5.
Appropriate correction is required.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5.1 Claim 1 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 of Patent No. 6465742 and in view of Okubora et al. (Patent # 6528732 hereinafter "Okubora") .

As to claim 1: The claim 1 of the instant application and claim 8 of Patent #6465742 are directed to a wiring substrate having an insulating substrate with a porous structure including continuous pores and wiring conductors selectively formed in the porous structure;

Claim 1 discloses continuous pores and claim 8 of Patent #6465742 teaches "the pores of the first and second porous bodies are through-holes". However, this limitation in claim 8 of Patent #6465742 still reads on claim 1 of application.
Claim 1 discloses "wiring conductors" and claim 8 of Patent #6465742 teaches " the two dimensional wiring pattern". However, this limitation in claim 8 of Patent #6465742 still reads on claim 1 of application.

except, claim 1 of Patent No. 6844504 does not discloses an electronic device module comprising an electronic device directly connected to said wiring conductors formed in the porous structure.

Okubora teaches in Fig. 8F an electronic device module comprising an electronic device 50 directly connected to said wiring conductors.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made to modify the patent's claimed invention by utilizing an insulating substrate with a porous structure to make an electronic device module comprising an electronic device directly connected to said wiring conductors formed in the porous structure.
Claim 1 correspond to claim 8 of patent #6844504.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6.1. Claims 1 is rejected under 35U.S.C. 103(a) as being obvious over Okubora in view of Sakamoto et al. (Patent #5103288 hereinafter "Sakamoto") and in view of Ohya et al. (Patent #5531945 hereinafter "Ohya").

As to claim 1: Okubora discloses in Fig. 8F an electronic device module comprising: a wiring substrate 43, Fig. 8B having an insulating substrate (41, Fig. 8 and column 5, lines 18-22) and wiring conductors 43b, 44, Fig. 8F selectively formed in substrate; and an electronic device 50 directly connected to said wiring conductors formed in the substrate.

except , Okubora doesn't explicitly teach a substrate with a porous structure.

Sakamoto discloses a substrate with a porous structure (column 2, lines 65-68 and column 3, lines 1-9).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention that a substrate with a porous structure as taught by Sakamoto because Sakamoto teaches that such structure would result in the benefit of reducing the parasitic capacitance.

However, Okubora doesn't explicitly teach a porous structure including continuous pores.

Ohya teaches a porous structure including continuous pores.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention that a porous structure including continuous pores, as taught by Ohya because Ohya teaches that such structure would result in the benefit of forming a printed wiring network.

Instant modified Okubora clearly teaches all of the claimed limitations and particularly "said wiring conductors". However, the examiner notes that a limitation "formed in the porous structure" is a process limitation in the product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP 2113 and 2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985). And further, if the prior art structure (Okubora as modified, disclosed wiring conductors) is capable of performing the intended use, then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) AND In re Otto, 136 USPQ 458, 459 (CCPA 1963). Therefore, at time the invention was made, it was well know to use wiring conductors formed in the porous structure.

6.2 Claims 1-4, 6 and 8-9 are rejected under 35U.S.C. 103(a) as being obvious over of Okubora in view Admitted by Applicant (Prior Art, hereinafter APA) .

As to claim 1: Okubora discloses in Fig. 8F an electronic device module comprising: a wiring substrate 43, Fig. 8B having an insulating substrate (41, Fig. 8 and column 5, lines 18-22) and wiring conductors 43b, 44, Fig. 8F selectively formed in substrate; and an electronic device 50 directly connected to said wiring conductors substrate.

except , Okubora doesn't explicitly teach a substrate with a porous structure including continuous pores.

APA discloses at time the invention was made, it was well know to use a three-dimensional structure of the substrate including continuous pores.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention that a substrate with a porous structure including continuous pores as taught by APA because APA teaches that such structure would result in the benefit of stereoscopic wiring board with high degree of freedom in circuit design.

Instant modified Okubora clearly teaches all of the claimed limitatio9ns and particularly "said wiring conductors". However, the examiner notes that a limitation "formed in the porous structure" is a process limitation in the product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP 2113 and 2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985). And further, if the prior art structure (Okubora as modified, disclosed wiring conductors) is capable of performing the intended use, then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) AND In re Otto, 136 USPQ 458, 459 (CCPA 1963). Therefore, at time the invention was made, it was well know to use wiring conductors formed in the porous structure.

As to claim 2: Okubora discloses the electronic device module according to claim 1, wherein said wiring conductors in the wiring substrate are grouped into a first wiring conductor 43a, 43b extending in parallel with a electronic device mounting surface of the porous insulating substrate (41, Fig. 8 and column 5, lines 18-22) and a second wiring conductor 44 extending through the porous insulating substrate from its top surface to bottom surface, Fig. 8B. We consider through hole 44 as a second wiring conductor because as taught by Okubora via-holes which are metal plated at the inner wall to give a level of conductivity or filled with an electrically conductive paste for yielding the via holes to connect between the patterns in layers (column 8, lines 40-49).

Notes: At time the invention was made, it was well know to create conductors from photosensitive layer. Shibasaki et al. (Patent #4296424 hereinafter "Shibasaki") teaches how to create conductors 3, 5a, 5b, Fig. 3 from photosensitive layer 2. The insulation substrate 1, Fig. 3, includes a photosensitive layer 2 that is, upon exposure to irradiated energy rays, exhibit conductive properties and forms electrodes, as recited Shibasaki (column 4, lines 27-41).

As to claim 3: Okubora discloses the electronic device module according to claim 2, wherein said first wiring conductor 72 Fig. 9E is formed at a surface of said wiring substrate 71.

As to claim 4: Okubora discloses the electronic device module according to claim 2, wherein said first wiring conductor (71a, 71b Fig. 9A and column 8, lines 51-55) is embedded in said wiring substrate 71.

As to claim 6: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 1, wherein the wiring substrate 49 and the electronic device 50 are directly connected with each other by bonding layers provided at contacts of the wiring conductors 44p with terminal electrodes 51 of the electronic device 50 Fig.8E.

As to claim 8: Okubora discloses the electronic device module according to claim 1, wherein a size of the electronic device 50 is smaller than the size of the wiring substrate 49, Fig.8E.

As to claim 9: Okubora discloses the electronic device module according to claim 1, wherein the insulating substrate 49 has almost the same coefficient of thermal expansion as that of the electronic device 50, (column 7, lines 36-49 column 11, lines 37-42)

6.3. Claim 5 is rejected under 35U.S.C. 103(a) as being obvious over Okubora in view of Shibasaki .

As to claim 5: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 2, wherein, in the junction of the first 43a and second wiring conductors defined as planes in parallel with the electronic device 50 mounting surface of the wiring substrate, Fig. 8F,

except, Okubora doesn't explicitly teach the second wiring conductor along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor.

Shibasaki discloses the second wiring conductor 3, 5a, 5b, Fig. 3 along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor. Shibasaki teaches (column 4, lines 27-41) the insulation substrate 1, Fig. 3, includes a photosensitive layer 2 that is, upon exposure to irradiated energy rays, exhibit conductive properties and forms electrodes. At time the invention was made, it was well know how to create conductors from photosensitive layer and that second wiring conductor along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention that the second wiring conductor along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor to provide compound module.

6.4. Claim 7 is rejected under 35U.S.C. 103(a) as being obvious over Okubora in view of Yasuda et al. (Patent 2002/0100610 hereinafter "Yasuda").

As to claim 7: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 1,

except, Okubora doesn't explicitly teach a size of the electronic device and a size of the wiring substrate are substantially the same.

Yasuda discloses in Fig. 4A a size of the electronic device 5 and a size of the wiring substrate 6 are substantially the same. At time the invention was made, it was well know to use
so-called chip size package (CSP), when a size of the electronic device and a size of the wiring substrate are substantially the same.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention a size of the electronic device and a size of the wiring substrate are substantially the same.

Benefit of doing so is to reduce size of the semiconductor devices.

6.5. Claims 10, 11 are rejected under 35U.S.C. 103(a) as being obvious over Okubora in view of Japp et al. (Patent #6722031, hereinafter "Japp")

As to claim 10: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 1,

except, Okubora doesn't explicitly teach the electronic device is of semiconductor chip, and the wiring substrate serves as a package base on which the semiconductor chip is mounted.

Japp discloses the electronic device is of semiconductor chip 160, Fig. 2, and the wiring substrate 1020 serves as a package base on which the semiconductor chip is mounted. At time the invention was made, it was well know to use the wiring substrate serves as a package base on which the semiconductor chip is mounted.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the electronic device is of semiconductor chip, and the wiring substrate serves as a package base on which the semiconductor chip is mounted .

Benefit of doing so is to prevent damage of the chip and provide necessarily connections.

As to claim 11: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 10,

except, Okubora doesn't explicitly teach the semiconductor chip that is mounted on a top surface of the package base, with its terminal electrodes facing downwards, and a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other

part of the wiring conductors extend to a bottom side of the package base.

Japp discloses in Fig. 2 the semiconductor chip 160 that is mounted on a top surface of the package base 1020, with its terminal electrodes 107 facing downwards, and a part of the wiring conductors 103 of the package base 1020 are directly coupled to the semiconductor chip 160, and other part of the wiring conductors 1006, 1008 extend to a bottom side of the package base. At time the invention was made, it was well know the semiconductor chip that is mounted on a top surface of the package base, with its terminal electrodes facing downwards.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the semiconductor chip that is mounted on a top surface of the package base, with its terminal electrodes facing downwards, and a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend to a bottom side of the package base.

Benefit of doing so is to provide connections of the chip with another printed circuit board.

6.6. Claim 12 is rejected under 35U.S.C. 103(a) as being obvious over Okubora in view of Japp and in view of Hur (Patent #6646334, hereinafter "Hur")

As to claim 12: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 10,

except, Okubora doesn't explicitly teach the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base, with its terminal electrodes facing upwards.

Hur teaches the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base with its terminal electrodes facing upwards. Therefore, at time the invention was made, it was well know the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base with its terminal electrodes facing upwards.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base with its terminal electrodes facing upwards.

Benefit of doing so is to provide possibility to use both sides of the substrate.

Okubora also fail to discloses that a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend at the bottom surface of the package base.

Japp discloses in Fig. 2 the semiconductor chip 160 that is mounted on a surface of the package base 1020,and a part of the wiring conductors 103 of the package base 1020 are directly coupled to the semiconductor chip 160, and other part of the wiring conductors 1006, 1008 extend to a bottom side of the package base. At time the invention was made, it was well know that a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend at the bottom surface of the package base.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base, with its terminal electrodes facing upwards, and a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend at the bottom surface of the package base.

Benefit of doing so is to provide connections of the chip with another printed circuit board.

7.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

7.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

7.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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